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Specification

1. Title of the Invention

SEMICONDUCTOR DEVICE

2. Scope of the claims

1. A semiconductor device having an intrinsic semiconductor substrate and a pair of impurity diffusion regions provided on a major surface of the intrinsic semiconductor substrate, in which the pair of impurity diffusion regions and an intrinsic semiconductor region between these impurity diffusion regions constitute a back-to-back diode, characterized in that a trap level is provided in the intrinsic semiconductor region.

2. The semiconductor device according to claim 1, characterized by comprising: a semi-insulating GaAs substrate; a pair of n^+-type diffusion regions provided on a major surface of the substrate; and a trap level formed in a surface portion of an intrinsic semiconductor region between the pair of n^+-type diffusion regions.

3. The semiconductor device according to claim 2, characterized in that the trap level of the intrinsic semi-insulating region is formed by electron beam irradiation and is about 0.1 to 0.2 eV.

3. Detailed Description of the Invention

[Field of the Industrial Application]

The present invention relates to a technology for manufacturing an n^+-i-n^+ protection diode to which a space-charge limited current to be generated on a semi-insulating conductor GaAs (gallium·arsenic) substrate is

applied, particularly relates to a technology for manufacturing a protection diode which is suitable for absorbing an electrostatic surge current of a GaAs MESFET (Metal Semiconductor Field Effect Transistor).

[Prior Art]

An n^+-i-n^+ diode is manufactured by providing a pair of n^+-type diffusion regions 2 and 3 on a major surface of a semi-insulating GaAs substrate 1, and then providing diode electrodes 5 and 6 on the n^+-type diffusion regions 2 and 3 that are not covered with an insulating film 4, as shown in Fig. 12. More specifically, a high-resistance semi-insulator (intrinsic semiconductor: i) with a resistivity of 10^7 to 10^8 ohm·cm is used for the semi-insulating GaAs substrate 1. As a result, an energy band diagram of the n^+-type diffusion regions 2 and 3 and an intrinsic semiconductor region (i-region) 7 between the n^+-type diffusion regions 2 and 3 is as shown in Fig. 13. In this energy band diagram, the part which is indicated by the dotted line is the Fermi level (FL), 8 denotes a conduction band, 9 denotes a valence band. And potential barriers a are formed at the interfaces between the n^+-type regions (n^+) and i-region. The potential barrier a is about 0.6 eV. Incidentally, the transitional region is called a space-charge limitation region b. In addition, the current(I)-voltage(V) characteristics of this diode are as shown in Fig. 14, and the withstand voltages are -Va and Va.

In such an n^+-i-n^+ diode, when a predetermined voltage is applied to the n^+-type diffusion regions 2 and 3, a current flows from the semi-insulating portion over the space-charge

limitation region b. This phenomenon is equivalent to that in a back-to-back type protection diode in which metallurgically manufactured n^+-p^+ diodes are joined in a back-to-back form. Therefore, it is known that the above described n^+-i-n^+ structure may become a protection diode which can be easily formed on a GaAs substrate (disclosed in Japanese Patent Laid-Open Publication No. Sho 61-292965).

[Problems to be solved by the Invention]

An n^+-i-n^+ diode can be formed simultaneously with formation of the n^+-type diffusion region which is formed when an FET is made on a GaAs substrate. Therefore, provision of p-diffusion region which is necessary for a protection diode formed by the use of p-n junction is unnecessary. Thus, an advantage is that the n^+-i-n^+ diode is easy to form.

However, it has been found by the present inventor that this diode is not high in surge absorbing ability (surge absorbing capacity) for the following reasons. That is, in an n^+-i-n^+ diode, a contact area between opposite n^+-type diffusion region and i-region cannot be set large because the depth of the diffusion layer of the n^+-type diffusion region is shallow. As a result, the cross-section for a flow-through surge current to pass through cannot be set large, and thus the surge absorbing ability falls short of that of the metallurgical bonded p-n diode.

In addition, it has been found that the heights of the potential barriers are prone to vary in this n^+-i-n^+ diode. That is, the potential barrier subtly changes with the deposition condition of the semi-insulating GaAs substrate, or the like.

Accordingly, the characteristics of the n^+-i-n^+ diode become prone to change.

An object of the present invention is to provide an n^+-i-n^+ diode which is high in surge absorbing ability.

Another object of the present invention is to provide a semiconductor device having an n^+-i-n^+ diode which is high in surge absorbing ability.

The above described and other objects and novel features will be apparent from the description of this specification and the attached drawings.

[Means for solving the Problems]

A brief description of an outline of a typical one out of the inventions disclosed in this application is as follows.

That is, in an n^+-i-n^+ diode of the present invention, a pair of n^+-type diffusion regions are provided on a major surface of a semi-insulating intrinsic GaAs substrate, and a back-to-back diode composed of n^+-i-n^+ is constituted. An i-region between the n^+-type diffusion region and n^+-type diffusion region is provided with a trap region having a trap level by irradiation of an electron beam. The trap level is located at 0.2 to 0.3 eV below a conduction band in the energy band. Accordingly, if this trap level is filled with electrons, a height of a potential barrier relative to the n^+-type diffusion region becomes 0.1 to 0.2 eV. This is sufficiently low in comparison with about 0.6 eV given in the case that the level does not exist.

[Effects]

According to the above described means, in the n^+-i-n^+

diode of the present invention, a trap level is formed in the i-region by electron beam irradiation. The trap level is located at 0.2 to 0.3 eV below a conduction band in the energy band. Accordingly, if this trap level is filled with electrons, a height of a potential barrier relative to the n^+-type diffusion region becomes 0.1 to 0.2 eV. This is sufficiently low in comparison with about 0.6 eV given in the case that the level does not exist. As a result, if a surge current (electrons) flows through the i-region, the initial electrons are trapped in the trap level in the i-region. Thereafter, the trap level is filled with electrons, and as a result, the energy level of the i-region approaches the energy level of the n^+-type diffusion region. In this manner, once the energy level of the i-region become close to that of the n^+-type diffusion region, the potential barrier for the subsequent surge current is lowered from 0.6 eV to between 0.1 and 0.2 eV. Therefore, the surge current easily flows from an n^+-type diffusion region into the other n^+-type diffusion region, and thus the surge absorbing capability becomes high.

[Embodiment]

Hereinafter, a description will be given of an embodiment of the present invention with reference to the drawings.

Fig. 1 is a sectional view showing a sketch of an n^+-i-n^+ diode in a GaAs MESFET with a protection diode according to an embodiment of the present invention; Fig. 2 is an energy band diagram of the same; Fig. 3 is an energy band diagram of the same in a state where a surge current flows; Fig. 4 is a graph showing current-voltage characteristics of the same before a

surge current starts to flow; Fig. 5 is a graph showing current-voltage characteristics of the same in a state where a surge current flows; Fig. 6 is a schematic plan view showing a sketch of the same FET; Fig. 7 is a equivalent circuit diagram of the same. Figs. 8 to 11 are sectional views of an n^+-i-n^+ diode in each manufacturing process. Fig. 8 is a sectional view showing a state where ion implantation into a major surface of a semi-insulating GaAs substrate is performed; Fig. 9 is a sectional view showing a semi-insulating GaAs substrate which has been subjected to diffusion treatment; Fig. 10 is a sectional view showing a semi-insulating GaAs substrate which is partially irradiated with an electron beam; Fig. 11 is a sectional view showing a semi-insulating GaAs substrate on which diode electrodes are formed.

In description of this embodiment, a description will be given of an example where the present invention is applied to a GaAs MESFET with a protection diode. The GaAs MESFET with the protection diode has a structure in which a back-to-back diode (protection diode) 10 is interposed between the gate and source of the MESFET including the gate (G), source (S), and drain (D) as shown in the equivalent circuit of Fig. 7. In GaAs MESFETs, a gate length of the device is shortened to 1 μm or less typically in order to enable fast operation, making use of the physical property that the electron mobility in GaAs is high in comparison to that in Si. Thus, the electrostatic discharge resistance is weakened. Therefore, in order to enhance the electrostatic discharge resistance, a high performance protection diode is provided between the gate and

source.

In a GaAs MESFET chip (semiconductor device) 20, a pattern for the source electrode, drain electrode, and gate electrode and the like is as shown in Fig. 6. Specifically, a pair of source and drain electrodes 21 and 22, which are formed in rectangular patterns, are provided on the major surface of the rectangular chip 20. In addition, a gate electrode 23 is elongated between the source and drain electrodes 21 and 22. A part of the gate electrode 23 outside the source and drain electrodes 21 and 22 is wide and forms a wire bonding portion 24. Also in the source and drain electrodes 21 and 22, wire bonding portions 25 and 26 are provided.

On the other hand, the protection diode 10, i.e. the n^+-i-n^+ diode 10 which is formed of n^+-i-n^+, is provided on the left side of the chip 20. This n^+-i-n^+ diode 10 is constituted of a pair of n^+-type diffusion regions 2 and 3, and an intrinsic semiconductor region (i-region) 7 between the n^+-type diffusion regions 2 and 3 as shown by dotted lines. In addition, this intrinsic semiconductor region 7 is also a trap region 27 which is formed by electron beam irradiation as shown by the chain double-dashed line. Moreover, diode electrodes 5 and 6 are provided on the n^+-type diffusion regions 2 and 3, respectively. One diode electrode 5 extends on the surface of the chip 20. This extending interconnection portion 28 is electrically connected to the source electrode 21. Furthermore, an interconnection portion 29 of the other diode electrode 6 is electrically connected to the gate electrode 23.

Next, the structure of the n^+-i-n^+ diode 10 will be

described in detail. That is, Fig. 1 is a sectional view showing the structure of the n^+-i-n^+ diode 10. The n^+-i-n^+ diode 10 is formed by providing the surface of the intrinsic semi-insulating GaAs substrate 1 with the pair of n^+-type diffusion regions 2 and 3. The semi-insulating GaAs substrate 1 is made of an intrinsic semiconductor whose resistivity ρ is 10^7 to 10^8 ohm·cm. On the other hand, the n^+-type diffusion regions 2 and 3 are made of an extrinsic semiconductor in which donors are implanted.

The n^+-type diffusion regions 2 and 3 are formed as follows. That is, as shown in Fig. 8, a SiO_2 film 31 is selectively provided on the major surface of the semi-insulating GaAs substrate 1 in a thickness of about 5000 angstrom. Subsequently, Si ions 32 are implanted using the SiO_2 film 31 as a mask, and annealing is performed. Consequently, the diffusion regions 2 and 3 are formed as shown in Fig. 9. The implantation of the Si ions 32 is performed at 150 KeV at a dose of 3×10^{13} cm^{-2}. The implanted Si ions 32 are activated by annealing in an atmosphere including As at 800°C for 20 minutes. The activated Si ions 32 diffuse to a depth of 0.1 to 0.2 μm to form the n^+-type diffusion regions 2 and 3. As a result, the sheet resistance of the n^+-type diffusion regions 2 and 3 are 100 to 150 ohm/square. In addition, the distance l between the n^+-type diffusion regions 2 and 3 is several micrometers.

By implanting the Si ions 32 into regions on the intrinsic semi-insulating GaAs substrate 1 which are separated by a predetermined distance, the basic form of the n^+-i-n^+ diode 10 using the semi-insulating GaAs substrate 1 as an i-region is

formed.

On the other hand, in this embodiment, the trap region 27 (region indicated by the dotted line) is provided in an i-region 7 between the pair of n^+-type diffusion regions 2 and 3 as shown in Fig. 1. Moreover, a trap level (electron trap level) 33 is formed as shown in the energy band diagram of Fig. 2. This trap level 33 is formed by irradiating the corresponding intrinsic semiconductor region 7 between the n^+-type diffusion regions 2 and 3 with an electron beam 34 as shown in Fig. 10. The irradiation of the electron beam is performed at an implantation energy of 0.7 to 2 MeV and a dose of 1×10^{12} to 1×10^{14} cm^{-2}. As a result, the trap region 27 having a depth of 0.2 to 0.4 ηm, which is about twice as large as those of the n^+-type diffusion regions 2 and 3, is formed. The trap level 33 of the trap region 27 is located at h eV below a conduction band 8, for example at 0.2 to 0.3 eV, as shown in the energy band diagram of Fig. 2. Incidentally, in the energy band diagram, the part which is indicated by the dotted line is the Fermi level (FL). Reference numeral 8 denotes the conduction band, and reference numeral 9 denotes a valence band. Furthermore, potential barriers a are formed at the interfaces between the n^+-type regions (n^+) and i-region. Because the forbidden band of the GaAs is 1.42 eV at 300K, and the conduction band 8 is located at about 1 eV above the Fermi level in the n^+-GaAs, the potential barrier a is about 0.6 eV. The transitional region is called a space-charge limitation region b. Incidentally, the irradiation of the electron beam is performed, in particular, to the i-region 7 for diode formation,

therefore other regions are not adversely affected by the irradiation.

In addition, on the n^+-type diffusion regions 2 and 3, the diode electrodes 5 and 6 are formed by the use of AuGe (gold and germanium) alloy as shown in Fig. 11. Therefore, the protection diode 11 is formed.

Next, a description will be given of the operation of such an n^+-i-n^+ diode 10. In this n^+-i-n^+ diode 10, the trap region 27 having the trap level 33 is provided in the intrinsic semiconductor region (i-region) 7 between the n^+-type diffusion regions 2 and 3. Consequently, the following effects are obtained. The energy band diagram of the n^+-i-n^+ diode with a conventional structure is as shown in Fig. 13 as described above. In this case, before and after a surge current begins to flow, the heights of the energy barrier are equal, i.e. about 0.6 eV. Therefore, the I-V characteristics of the conventional diode do not change as shown in Fig. 14.

On the other hand, in the energy band diagram of the n^+-i-n^+ diode 10 of the present invention, the trap level 33 is present in the i-region 7. Although the trap level 33 is present in the i-region 7 until immediately before a surge current begins to flow as shown in Fig. 2, the energy barrier is a, i.e. about 0.6 eV as in the case of the conventional structure. Accordingly, the I-V characteristics at the moment when a surge current begins to flow are as shown in Fig. 4, which are the same as those of the conventional case shown by Fig. 14. That is, the n^+-i-n^+ diode 10 of the present invention has a withstand voltage equal to that of conventional one unless a surge current

flows, and no bad influence is exerted on the MESFET to which the protection diode 10 is connected, as in the case of the conventional one.

On the other hand, once a surge current begins to flow, electrons 35 are trapped in the trap level 33 in the i-region 7, and the energy band diagram becomes one which is shown in Fig. 3. Consequently, the potential barrier d is lowered to a value of the order of 0.1 to 0.2 eV. As shown in Fig. 5, the I-V characteristics corresponding to this state have a lower diode withstand voltages V_R' ($V_R' < V_R$) and $-V_R'$ ($-V_R' > -V_R$) in comparison with those in the I-V characteristics in a state before a surge current begins to flow. As a result, it is easy for a current to flow through the n^+-i-n^+ part for the subsequent surge current. Thus, according to the structure of the present invention, even the n^+-i-n^+ diode 10 having a small facing area of the n^+-type diffusion regions 2 or 3 and the i-region 7 can function as a diode with a high surge absorbing ability.

According to such an embodiment, effects as described below will be achieved.

(1) In the n^+-i-n^+ diode of the present invention, the intrinsic semiconductor region is the trap region having the trap level. Once a surge current begins to flow, the potential barrier relative to the n^+-type diffusion region of the intrinsic semiconductor region is lowered from 0.6 eV to between 0.1 and 0.2 eV. Thus, it is easy for the subsequent surge current to flow, and an effect that the surge absorbing ability becomes high as in the case of the p-n junction diode can be achieved.

(2) As a result of the effect (1) as described above, the surge absorbing ability of the n^+-i-n^+ diode of the present invention becomes high, and thus an effect that the electrostatic discharge resistance of a MESFET increases can be achieved.

(3) According to the present invention, the trap level is formed by electron beam irradiation of which controllability is good, thus an effect that, even if the potential barrier of the semi-insulating GaAs substrate changes, a desired trap level can be formed with a good reproducibility can be achieved.

(4) As a result of the effect (3) as described above, according to the present invention, the trap level can be formed with a good reproducibility, thus an effect that the characteristics of the n^+-i-n^+ diode become stable can be achieved.

(5) As a result of the effect (4) as described above, according to the present invention, the trap level can be formed with a good reproducibility, thus an effect that the yield improves can be achieved.

(6) As a result of the effects (1) to (5) as described above, according to the present invention, a synergistic effect that it is possible to provide the n^+-i-n^+ diode which is excellent in surge absorbing ability and, at the same time, to provide the GaAs MESFET with a protection diode which is inexpensive and has a high electrostatic discharge resistance can be achieved.

The invention made by the present inventor has been specifically described above on the basis of the embodiment. However, the present invention is not limited to the above described embodiment, and various changes are possible without

departing from the gist thereof, of course. For example, even when another semiconductor other than GaAs is used for the intrinsic semiconductor substrate, similar effects as in the above described embodiment can be achieved. In this case, in Si, even in an intrinsic semiconducting state, electrons are easy to flow, and thus it is necessary to put some thought into designing a circuit.

In addition, although the trap level 33 is formed by electron beam irradiation in the above described embodiment, the trap level 33 may be formed by plasma irradiation, neutron irradiation, or the like.

In the above description, a case that the invention made by the present inventor is applied to a technology for manufacturing a GaAs MESFET with a protection diode which pertains to the field of application that is the background of the present invention, has been explained. However, the present invention is not limited to this, and is applicable to a technology for manufacturing a GaAs IC and the like.

The present invention can be applied at least to manufacturing a semiconductor device incorporating an n^+-i-n^+ diode.

[Effects of the Invention]

A brief explanation for the effects which are achieved by the typical one of the invention disclosed in the present application is as follows.

In the n^+-i-n^+ diode of the present invention, since an electron trap level formed by electron beam irradiation is provided in an intrinsic semiconductor region, which is

semi-insulating high-resistance region, the trap level is filled with electrons when a surge current flows through the n^+-i-n^+ part of the diode. Therefore, the height of the potential barrier of the intrinsic semiconductor region relative to that of the n^+-type diffusion region becomes small. Therefore, according to the present invention, the tolerance to flowing-through of a surge current is enhanced, and the performance of a protection diode against electrostatic discharge damage can be improved.

4. Brief Description of the Drawings

Fig. 1 is a sectional view showing a sketch of an n^+-i-n^+ diode in a GaAs MESFET with a protection diode according to an embodiment of the present invention;

Fig. 2 is an energy band diagram of the same;

Fig. 3 is an energy band diagram of the same in a state where a surge current flows;

Fig. 4 is a graph showing current-voltage characteristics of the same before a surge current starts to flow;

Fig. 5 is a graph showing current-voltage characteristics of the same in a state where a surge current flows;

Fig. 6 is a schematic plan view showing a sketch of the same FET;

Fig. 7 is an equivalent circuit diagram of the same;

Fig. 8 is a sectional view showing a state where ion implantation into a major surface of a semi-insulating GaAs substrate is performed in manufacturing the n^+-i-n^+ diode;

Fig. 9 is a sectional view showing a semi-insulating GaAs substrate which has been subjected to diffusion treatment in

manufacturing the same;

Fig. 10 is a sectional view showing a semi-insulating GaAs substrate which is partially irradiated with an electron beam;

Fig. 11 is a sectional view showing a semi-insulating GaAs substrate on which diode electrodes are formed;

Fig. 12 is a sectional view showing a sketch of a conventional n^+-i-n^+ diode;

Fig. 13 is an energy band diagram of the same; and

Fig. 14 is a graph showing current-voltage characteristics of the same.

1...semi-insulating GaAs substrate, 2 and 3...n^+-type diffusion region, 4...insulating film, 5 and 6...diode electrode, 7...intrinsic semiconductor region (i-region), 8...conduction band, 9...filled band, 10...n^+-i-n^+ diode (protection diode), 20...chip, 21...source electrode, 22...drain electrode, 23...gate electrode, 24...wire bonding portion, 25 and 26...wire bonding portion, 27...trap region, 28...interconnection portion, 29...interconnection portion, 31...SiO_2 film, 32...Si ion, 33...trap level, 34...electron beam, 35...electron

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